

CLC5526 Digital Variable Gain Amplifier (DVGA)

Check for Samples: [CLC5526](#)

FEATURES

- **350 MHz Bandwidth**
- **Differential Input and Output**
- **Gain Control: Parallel w/data Latching**
- **Supply Voltage: +5V**
- **Supply Current: 48 mA**

KEY SPECIFICATIONS

- **Low Two Tone Intermod:**
 - **Distortion: –64 dBc @ 1 VPP, 150 MHz**
 - **24.5 dBm IP3, 150 MHz**
- **Low Noise: 2.5 nV/√Hz (Max Gain), 9.3 dB Noise Figure (Max Gain)**
- **Wide Gain Range: +30 dB to –12 dB**
- **Gain Step Size: 6 dB**

APPLICATIONS

- **Cellular/PCS Base Stations**
- **IF Sampling Receivers**
- **Infrared/CCD Imaging**
- **Back-channel Modems**
- **Electro-optics**
- **Instrumentation**
- **Medical Imaging**
- **High Definition Video**

DESCRIPTION

The CLC5526 is a high performance, digitally controlled, variable-gain amplifier (DVGA). It has been designed for use in a broad range of mixed signal and digital communication applications such as mobile radio, cellular base stations and back-channel modems where automatic-gain-control (AGC) is required to increase system dynamic range.

The CLC5526 has differential input and output, allowing large signal swings on a single 5V rail. The input impedance is 200Ω. The differential output impedance is 600Ω and is designed to drive a 1 kΩ differential load. The output amplifier has excellent intermodulation performance. The CLC5526 is designed to accept signals from RF elements and maintain a terminated impedance environment.

The CLC5526 maintains a 350 MHz bandwidth over its entire gain and attenuation range from +30 dB to –12 dB. Internal clamping ensures very fast overdrive recovery. Two tone intermodulation distortion is excellent: at 150 MHz, 1 V_{pp} it is –64 dBc.

Input signals to the CLC5526 are scaled by an accurate, differential R-2R resistive ladder with an input impedance of 200Ω. A scaled version of the input is selected under digital control and passed to the internal amplifier. The input common mode level is set at 2.4V via a bandgap referenced bias generator which can be overridden by an external input.

Following the resistive ladder is a fixed, 30 dB gain amplifier. The output stage common mode voltage of the CLC5526 is set to 3V, by internal, positive supply connected resistors.

Digital control of the CLC5526 is accomplished by a 3-bit parallel gain control input and a data valid pin to latch the data. If the data is not latched, the DVGA is transparent to gain control updates. All digital inputs are TTL/CMOS compatible.

A shutdown input reduces the CLC5526 supply current to a few mA. During shutdown, the input termination is maintained and current attenuation settings are held.

The CLC5526 operates over the industrial temperature range of –40°C to +85°C. The part is available in a 20-pin SSOP package.



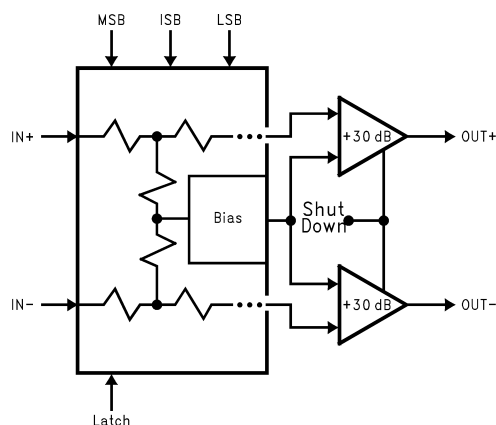
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

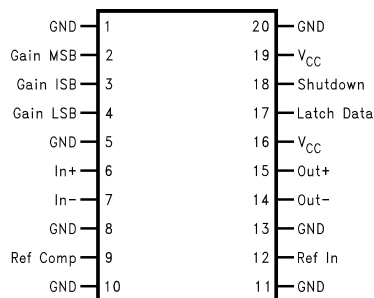
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

Block Diagram



Pin Configuration



Pin Descriptions

Pin Name	Pin No.	Description
GND	1, 5, 8, 10, 11, 13, 20	Circuit ground.
Gain MSB	2	Gain Selection Most Significant Bit
Gain ISB	3	Gain Selection Data Bit
Gain LSB	4	Gain Selection Least Significant Bit
In+	6	Positive Differential Input
In-	7	Negative Differential Input
Ref Comp	9	Reference Compensation
V _{CC}	16, 19	Positive Supply Voltage
Shutdown	18	Low Power Standby Control (Active High)
Latch Data	17	Data Latch Control (Active High)
Out+	15	Positive Differential Output
Out-	14	Negative Differential Output
Ref In	12	External Reference Input



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Positive Supply Voltage (V_{CC})	–0.5V to +6V
Differential Voltage between any two Grounds	<200 mV
Analog Input Voltage Range	–0.5V to + V_{CC}
Digital Input Voltage Range	–0.5V to + V_{CC}
Output Short Circuit Duration (one-pin to ground)	Infinite
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

- (1) “Absolute Maximum Ratings” are limited values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Positive Supply Voltage (V_{CC})	+5V ±5%
Differential Voltage between any two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	±0.5V
Operating Temperature Range	–40°C to +85°C

Package Thermal Resistance

Package	(θ_{JA})	(θ_{JC})
20-Pin SSOP	90°C/W	38°C/W

Reliability Information

Transistor Count	300
------------------	-----

Electrical Characteristics

The following specifications apply for $V_{CC} = +5V$, $R_L = 1\text{ k}\Omega$ maximum gain setting. **Boldface limits apply for $T_A = T_{min} = -40^\circ\text{C}$ to $T_{max} = +85^\circ\text{C}$, all other limits $T_A = 25^\circ\text{C}$** ⁽¹⁾⁽²⁾⁽³⁾.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
BW	Small-Signal Bandwidth			350		MHz
NOISE AND DISTORTION						
	2nd Harmonic Distortion	$f_{IN} = 150\text{ MHz}, 1\text{ V}_{PP}$	53	67		dBc
		$f_{IN} = 250\text{ MHz}, 1\text{ V}_{PP}$		64		dBc
		$f_{IN} = 150\text{ MHz}, 2\text{ V}_{PP}$	43	62		dBc
		$f_{IN} = 250\text{ MHz}, 2\text{ V}_{PP}$		58		dBc
	3rd Harmonic Distortion	$f_{IN} = 150\text{ MHz}, 1\text{ V}_{PP}$	53	71		dBc
		$f_{IN} = 250\text{ MHz}, 1\text{ V}_{PP}$		70		dBc
		$f_{IN} = 150\text{ MHz}, 2\text{ V}_{PP}$	43	57		dBc
		$f_{IN} = 250\text{ MHz}, 2\text{ V}_{PP}$		56		dBc

- (1) Limits are 100% tested at 25°C.
- (2) Typical specifications are the mean values of the distributions of deliverable amplifiers tested to date.
- (3) Outgoing quality levels are determined from tested parameters.

Electrical Characteristics (continued)

The following specifications apply for $V_{CC} = +5V$, $R_L = 1\text{ k}\Omega$ maximum gain setting. **Boldface limits apply for $T_A = T_{min} = -40^\circ\text{C}$ to $T_{max} = +85^\circ\text{C}$** , all other limits $T_A = 25^\circ\text{C}$ ⁽¹⁾⁽²⁾⁽³⁾.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IMD	Two Tone Intermodulation Distortion	$f_1 = 149.9\text{ MHz}$, $f_2 = 150.1\text{ MHz}$, 1 V_{PP} Composite		64		dBc
		$f_1 = 149.9\text{ MHz}$, $f_2 = 150.1\text{ MHz}$, 2 V_{PP} Composite		61		dBc
		$f_1 = 249.9\text{ MHz}$, $f_2 = 250.1\text{ MHz}$, 1 V_{PP} Composite		63		dBc
		$f_1 = 249.9\text{ MHz}$, $f_2 = 250.1\text{ MHz}$, 2 V_{PP} Composite		54		dBc
	Two Tone, 3rd Order Intermodulation	150 MHz		24.5		dBm
	Thermal Noise	Minimum Gain Setting		2.2		nV/ $\sqrt{\text{Hz}}$
		Maximum Gain Setting		2.5		nV/ $\sqrt{\text{Hz}}$
	Noise Figure	Maximum Gain Setting		9.3		dB
ANALOG I/O						
	Differential Input Impedance			200		Ω
	Differential Output Impedance			600		Ω
	Input Signal Level (AC Coupled)	Maximum Gain		126		mV
	Maximum Input Signal Level	Recommended		6		V_{PP}
	Maximum Output Signal Level	Recommended		4		V_{PP}
	Output Clipping			8		V_{PP}
GAIN PARAMETERS						
	Maximum Gain			30		dB
	Minimum Gain			-12		dB
	Gain Step Size			6.02		dB
	Gain Step Accuracy	(1 sigma)		0.03		dB
	Cumulative Gain Step Error	(1 sigma)		0.085		dB
DIGITAL INPUTS/TIMING						
	Logic Compatibility			TTL/CMOS		V
V_{IL}	Logic Input Low Voltage				0.8	V
V_{IH}	Logic Input High Voltage		2.0			V
T_{SU}	Setup Time			3		ns
T_{HOLD}	Hold Time			3		ns
T_{PW}	Minimum Pulse Width			3		ns
POWER REQUIREMENTS						
I_{CC}	+5V Supply Current			48	60	mA
	Shutdown			9		mA

Typical Performance Characteristics

($V_{CC} = +5V$, $R_L = 1\text{ k}\Omega$, max gain; unless specified)

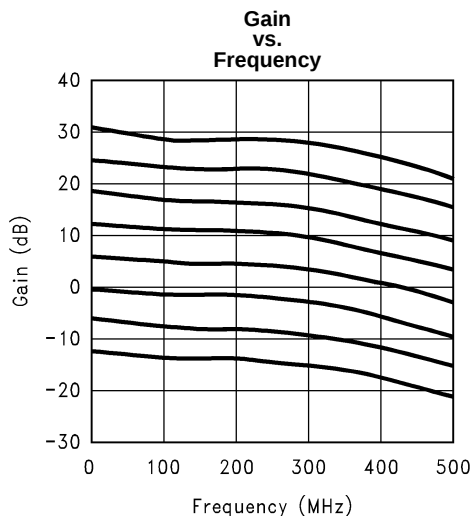


Figure 1.

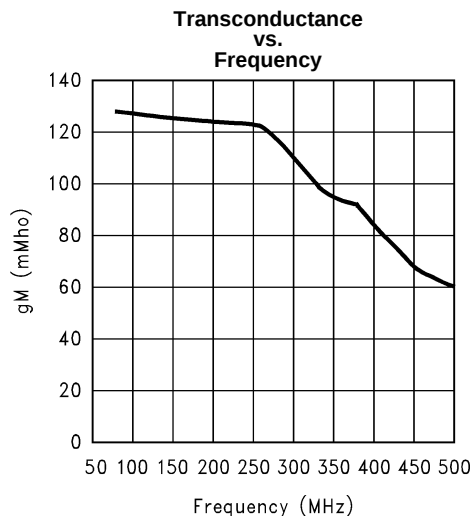


Figure 2.

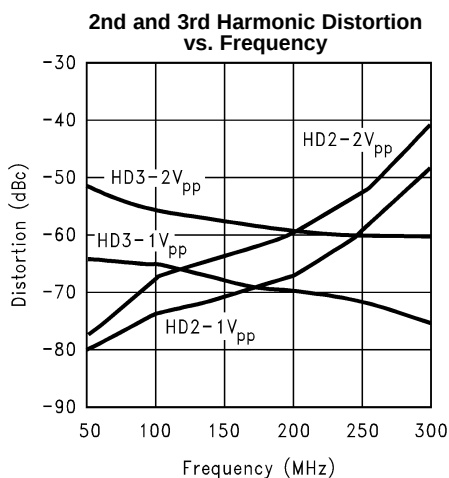


Figure 3.

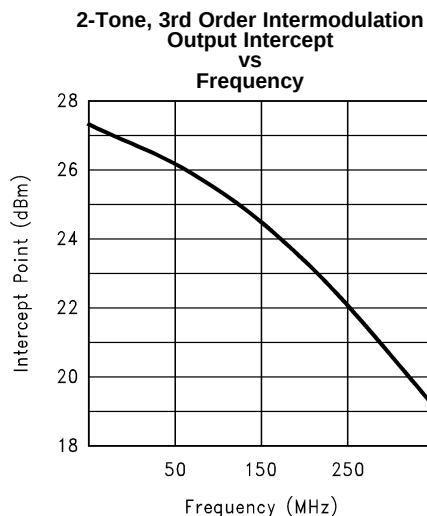


Figure 4.

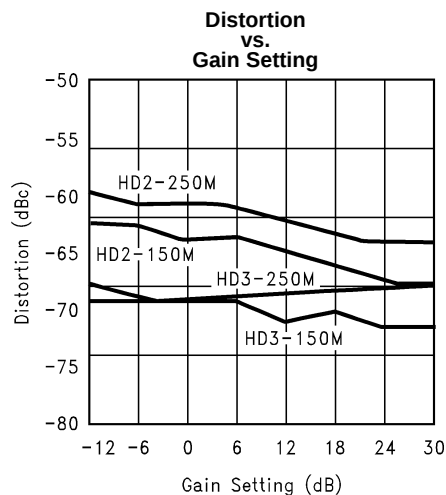


Figure 5.

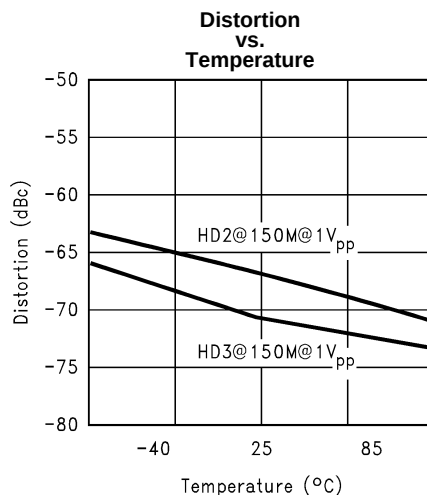


Figure 6.

Typical Performance Characteristics (continued)

($V_{CC} = +5V$, $R_L = 1\text{ k}\Omega$, max gain; unless specified)

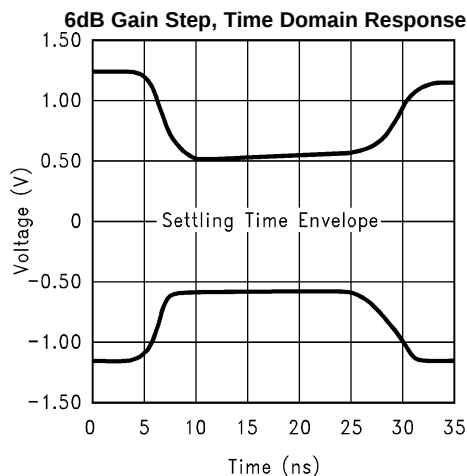


Figure 7.

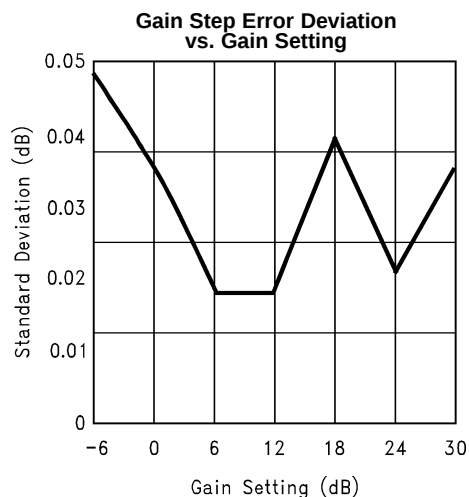


Figure 8.

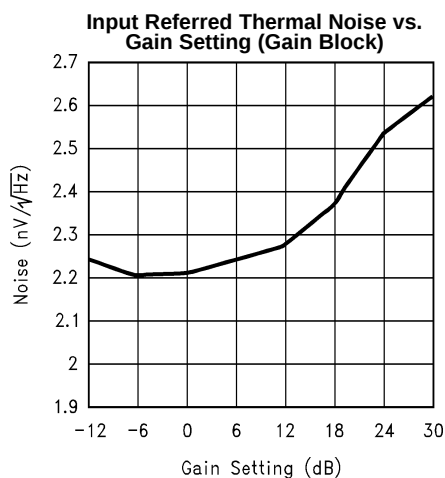


Figure 9.

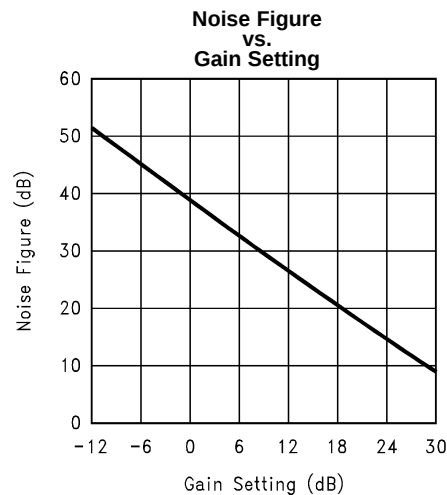


Figure 10.

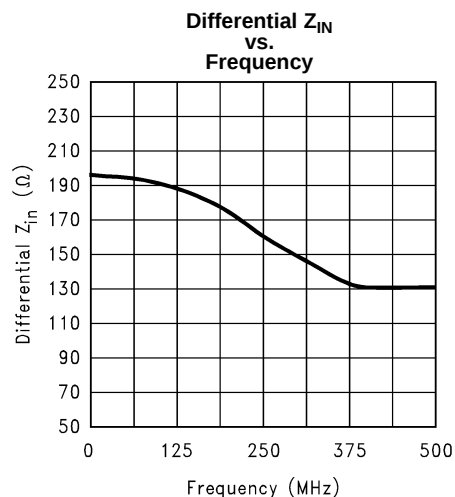


Figure 11.

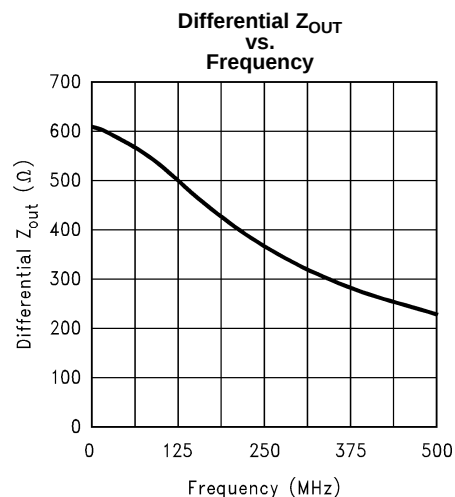
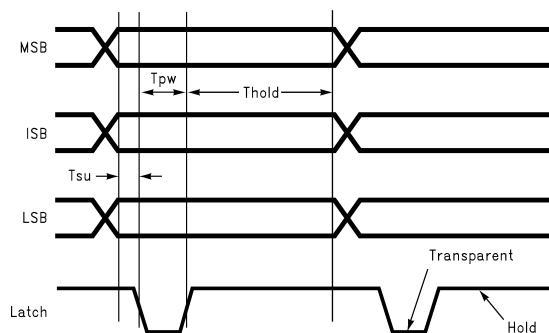


Figure 12.

Timing Diagram



Truth Table

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	-12
1	0	0	1	-6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

APPLICATIONS

DESCRIPTION

The CLC5526 is a digitally programmable, variable gain amplifier with the following features:

- 8 gain settings ranging from –12 to +30 dB in 6dB steps
- Differential inputs and outputs (externally AC coupled)
- Self biased input common-mode voltage
- 3-bit parallel digital control
- Single +5V supply
- Low-Power standby mode

Please refer to [Figure 13](#) for a representative block diagram.

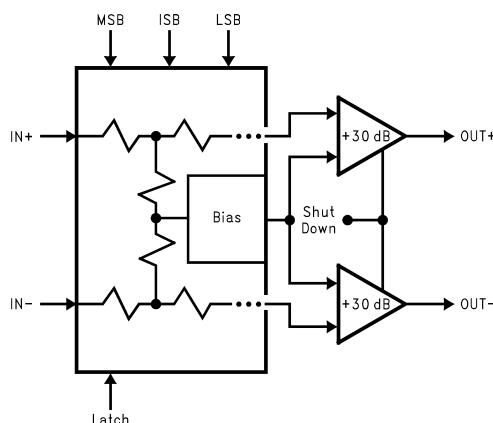


Figure 13. CLC5526 Block Diagram

GAIN SELECTION

Gain levels can be decreased from the maximum value in –6dB steps via the 3-bit digital inputs. [Table 1](#) shows the gain selection truth table for a 1000Ω differential load.

Table 1. Gain Selection Truth Table

Gain Word	MSB	ISB	LSB	Gain (dB)
0	0	0	0	–12
1	0	0	1	–6
2	0	1	0	0
3	0	1	1	+6
4	1	0	0	+12
5	1	0	1	+18
6	1	1	0	+24
7	1	1	1	+30

Gain settings can be calculated as follows:

$$\text{GAIN} = -12 \text{ dB} + (\text{Gain Word}) * 6.02 \text{ dB} \quad (1)$$

Gain selection has two modes: Transparent or latched, depending on the LATCH input. If the LATCH input is held LOW, then the device is in the transparent mode. Changes on data inputs will result in direct changes to the gain setting.

Input data will be latched upon the LOW to HIGH transition of LATCH. While LATCH is HIGH, digital data will be ignored until LATCH is strobed low again.

Note: Upon power-up the analog inputs are disconnected from the internal amplifier. LATCH will need to be strobed LOW before an analog output will be present!

DIFFERENTIAL I/O CONSIDERATIONS

Analog inputs and outputs need to be AC coupled to prevent DC loading of the common-mode voltages. If driving the CLC5526 from a single-ended 50Ω source is required, a 1:2 transformer should be used to generate the differential inputs. As the differential input impedance of the CLC5526 is 200Ω, the 1:4 impedance ratio will allow for optimum matching to the 50Ω source. The secondary outputs of the transformer should be AC coupled to the CLC5526 analog inputs, while the secondary center tap of the transformer should be directly connected to the system ground.

The CLC5526 is designed to drive differential circuits, such as the CLC5957 Analog to Digital convertor. Figure 14 below shows a typical application of the CLC5526.

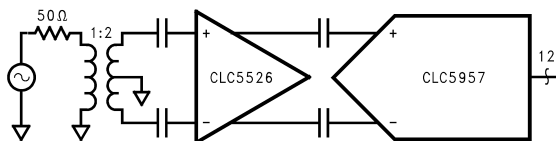


Figure 14. Differential I/O Connections

DRIVING LOADS

Actual gain of the CLC5526 will vary with the output load. The device is designed to provide +30 dB maximum gain with a 1000Ω differential load.

Each output of the CLC5526 contains an internal 300Ω resistor to the V_{CC} rail. Actual gain calculations need to take this in account with a given external load resistor. The effective load resistance can be used with the following equation to calculate max gain values.

$$A_V = 20 \log (0.0843 \cdot R_{\text{leff}})$$

where

- $R_{\text{leff}} = R_{\text{int}} \parallel R_{\text{ext(diff)}}$
- $R_{\text{int}} = 600\Omega$ differential

(2)

Figure 15 shows maximum gain values over output load. Resistor values are for differential loads.

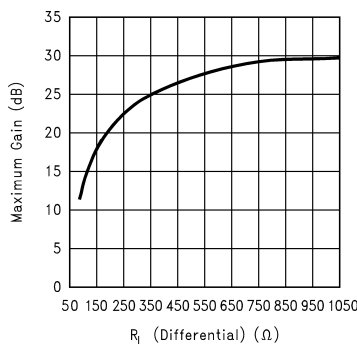


Figure 15. Maximum Gain vs R_{LOAD}

Stray capacitance at the output, along with the output load value will form a pole, which can degrade the CLC5526 bandwidth. For a narrow-band application this problem can be alleviated by using a tuned load, which will incorporate any stray parasitic impedance into a resonant circuit. By tuning the resonant load, full gain can be achieved with a given resistive load.

A typical tuned load is shown below in Figure 16, where the resonant frequency is tuned about 150 MHz.

The 1000Ω load in this circuit can represent the input impedance of the CLC5957 Analog to Digital converter. Actual values for the reactive components may vary slightly to account for board and device parasitic elements.

The Diversity Receiver Chipset may also use the ADC12L066 A/D converter in place of the CLC5957. Please refer to the Low Power Diversity Receiver Chipset (LDRCS) User's Guide for input matching between the CLC5526 and ADC12L066.

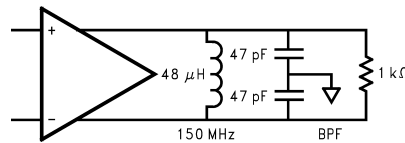


Figure 16. CLC5526 Driving a Tuned Load

Typical Application

Although the CLC5526 can be used as a general purpose digital variable gain amplifier, it was specifically designed to provide the variable gain function in TI's Diversity Receiver Chipset. In this application, the CLC5526 drives a tuned BPF and the CLC5957 Analog to Digital converter. Digitized IF data is downsampled and tuned with the CLC5903 dual digital tuner which also provides the AGC control function. AGC data is fed back to the CLC5526. The CLC5957 differential input impedance is 1000Ω, so with the tuned load, full gain of the CLC5526 is achieved. [Figure 17](#) shows the block diagram of the Diversity Receiver Chipset application. [Figure 18](#) shows the SINAD vs Input Power of the diversity receiver chipset. For input power levels ranging from 0 dB to -110 dB, the chip set provides a signal to noise ratio in excess of the 9 dB required for a typical GSM system.

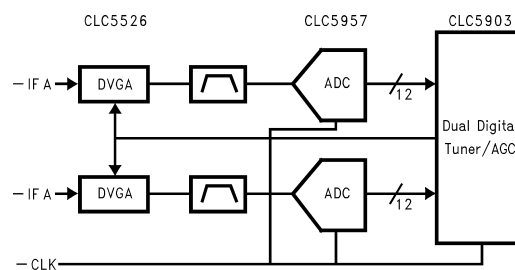
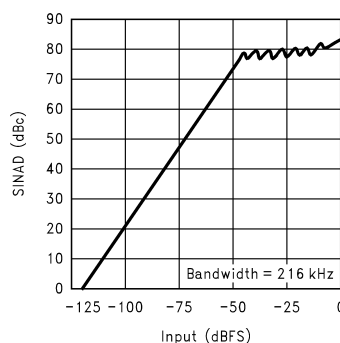


Figure 17. Diversity Receiver Chipset Block Diagram



**Figure 18. Diversity Receiver Chipset
SINAD vs Input Power**

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Texas Instruments provides evaluation boards for the CLC5526, which include input and output transformers for impedance matching and single to differential signal conversion.

Supply bypassing is required for best performance. Provide a 6.8 μF Tantalum and 0.1 μF ceramic capacitor as close as possible to the supply pin.

In addition, a 100 pF ceramic capacitor should be placed between the COMP pin (pin 9) and the system ground. This will filter high frequency noise from the common-mode level.

Ceramic coupling capacitors should be used to AC couple both the input and output. Actual values will depend upon the signal frequency.

Evaluation Board Layout and Schematic Diagram

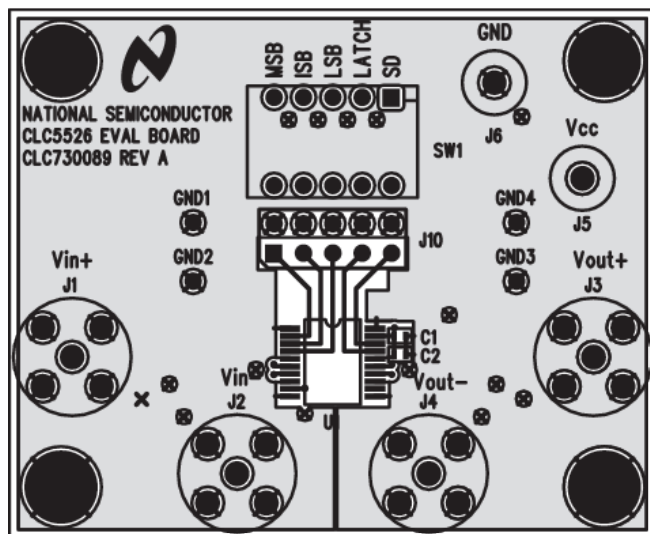


Figure 19. CLC5526 Layer 1

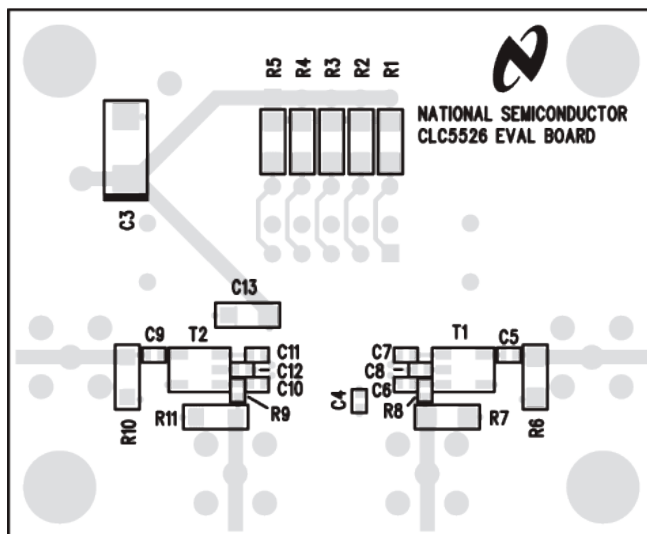


Figure 20. CLC5526 Layer 2

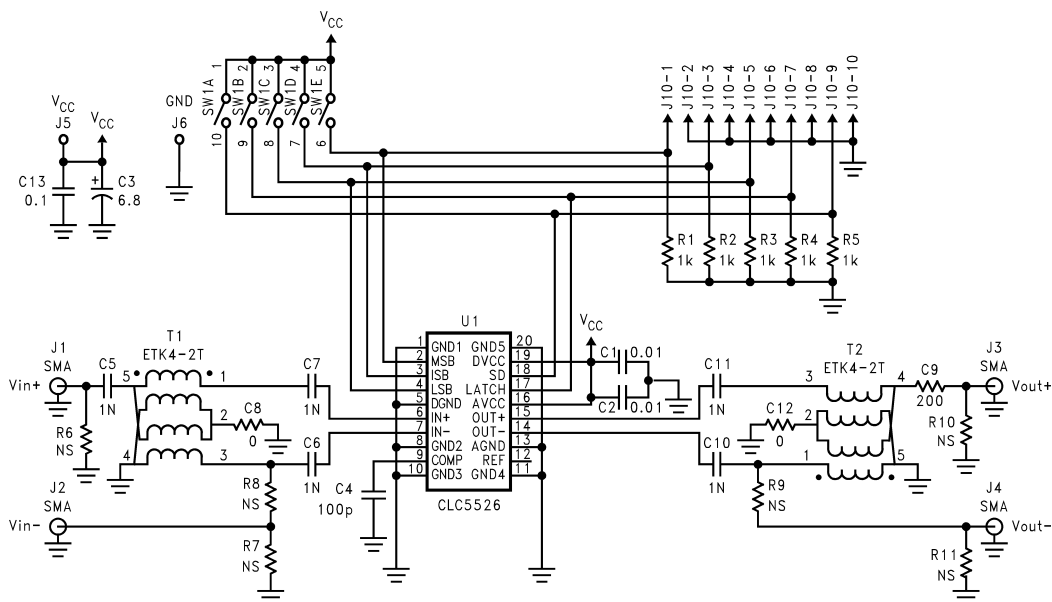


Figure 21. Evaluation Board Schematic

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E

Page

- Changed layout of National Data Sheet to TI format [11](#)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com